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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,568	02/25/2002	Stephen M. Gates	YOR919980324 US2	9141

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,568	GATES ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- Th MAILING DATE of this communication appears on th cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18 and 26-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18, 26-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 32 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 32 depends on base claim 38. The base claim 38 is disclosed a semiconductor device structure of Fig. 5B or Fig. 6B. However, none of Figs. 5B and 6B disclose the semiconductor node forming a part of a field effect transistor. Therefore, the limitation "..., said at least one semiconductor node forming a part of said at least one field effect transistor (claim 32)" is not supported by the original disclosure.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-12, 15-16, 18, 26, 28-29, 32-33 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319).

With respect to claims 11-12, 18, 26, 28-29, 33 and 38, Durlam's first embodiment

(Figs. 5-8) discloses an array of microelectronic elements comprising: a substrate of semiconductor material 11; a lower layer of dielectric material (12a,21,25) disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated conducting regions (19a,37) and (19b,38) (Fig. 5) disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material 51 disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of nodes (43,45) and (44,46) comprising MTJs 43 and 44 and disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor 19a and a via 37 formed on the metal conductor 19a and comprising a diffusion barrier material of Ta (not illustrated, see column 3, lines 35-42). It is noted that because the via 37 comprising the diffusion barrier material and because the via 37 extending between the metal conductor 19a and a node (43,45) in the plurality of nodes, the diffusion barrier material would also extend between the metal conductor 19a and the node (43,45) and electrically connecting the metal conductor 19a with the node (43,45).

Durlam's first embodiment does not disclose the plurality of nodes including semiconductor diodes.

However, Durlam further teaches a second embodiment of MRAM (Fig. 17)

having a plurality of nodes which include diodes 93 and 95 in contact with the conducting regions 82 at the upper surface of the lower layer. Accordingly, it would have been obvious to modify the first embodiment by forming the plurality of nodes with the structure as suggested by the second embodiment for the purpose of switching a magnetic memory element to read information in the magnetic memory element (column 6, lines 26-30).

With respect to claims 15-16, Durlam (Fig. 8) further discloses that the device comprises a field effect transistor 12a, a first insulating layer 54 is disposed over an upper surface of the upper layer, and a second insulating layer 33 is formed over the upper surface of the lower layer.

Regarding claim 32, it would have been obvious to form the semiconductor node of Durlam as a field effect transistor because it is an intended use depending upon the application which is desired for the semiconductor node of Durlam.

Regarding claims 36-37, Durlam's Fig. 7 further discloses a bonding promoting layer 33 of dielectric material formed on the lower layer 25 of dielectric material, the bonding promoting layer 33 bonding the lower surface of the upper layer 51 of dielectric material to the upper surface of the lower layer 33. As taught by Durlam, the bonding promoting layer 33 is placed between the lower layer 25 and the upper layer 51 to provide electrical isolation between the conductor layers (column 3, lines 60-64). Therefore, it would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers. It is noted that the process limitation (softening temperature in a

range of 400 degrees C to 500 degrees c) would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

4. Claims 13-14, 17, 27 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Bronner et al (US. 6,242,770).

Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4).

5. Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Oda (US. 5,994,749).

Durlam's first embodiment (**Figs. 5-8**) does not specifically disclose the metal conductor 19a being formed of a different material than the via 37.

However, Oda (Fig. 5) teaches the forming of a conventional conductive contact structure comprising an aluminum layer 114 in electrical contact with the via 118 made of tungsten (column 1, lines 28-36). Accordingly, it would have been obvious to form the metal conductor 19a and the via 37 of Durlam with the materials as set forth above because as taught by Oda, such materials are well known materials which are used for the wirings in a conductive contact structure.

Response to Arguments

6. Regarding claim 32, Applicant argues that "the invention of claim 32 is clearly disclosed at page 18, line 3 – page 9, line 2, and is clearly illustrated in Fig. 7 of the present Application."

The Examiner recognizes that Fig. 7 discloses a semiconductor device having a plurality of conductive regions connecting to a field effect transistor. However, Fig. 7 does not disclose a conductive region structure recited in the **base claim 38**. For example, Fig. 7 does not disclose "... a conductive via comprising a diffusion barrier material formed on said metal conductor; a second dielectric layer which is bonded to said first dielectric layer; and at least one semiconductor node formed in said second dielectric layer, said at least one semiconductor node being formed on and contacting said at least one conductive region, wherein said diffusion barrier material extends between said metal conductor and said at least one semiconductor node and electrically connects said metal conductor to said at least one semiconductor node (claim 38)." Therefore, Fig. 7 does not support the structure recited in claim 32 because claim 32 depends on base claim 38.

Applicant argues that Durlam does not disclose a "diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node" as recited in the base claims.

This argument is not persuasive because Durlam's Fig. 7 clearly discloses a via 37 formed on a metal conductor 19a and extending between the metal conductor 19a and a node (45,43) in the plurality of nodes. And because the via 37 including a

diffusion barrier material (column 3, lines 36-42), the diffusion barrier material would also extend between the metal conductor 19a and the node (45,43) in the plurality of nodes.

Applicant further argues that the diffusion barrier material of Durlam has a function which is completely different than the function of the diffusion barrier material in the claimed invention.

This argument is not persuasive because the reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by Applicant. *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972).

In response to Applicant's arguments regarding the Bronner reference and the Oda reference, the Examiner's arguments with respect to the Bronner reference and the Oda reference in the last Office action are herein incorporated by reference.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
February 5, 2004

PHAT X. CAO
PRIMARY EXAMINER